REMARKS

Claims 15 to 29 are now pending.

Applicants respectfully request reconsideration of the present application in view of this response.

35 U.S.C. § 102(e) – Davis reference

Claims 15 to 29 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,633,930 to Davis et al. ("Davis reference").

The Davis reference purportedly concerns a stored value transaction system having a plurality of value storing transfer devices, including at least a local device, a collection device, a consolidation device and a settlement device. Specifically, the Davis reference at cols. 10 to 11, appears to describe security functions of its device, reciting: "...all interaction between the SVC 20 and a reader/writer processor 74 begins with a dual-challenge, cross-verification procedure to establish a secure session as a result of positive confirmation that both the SVC 20 and the terminal (security module 78) are validated for the performance of a financial or other transaction. The secure session is established utilizing data stored within the memory of the SVC 20 and the memory of the security module 78...." and "[a] secure session is established in the present invention by separate encryption of certain data by both the SVC 20 and the security module 78 utilizing, in the present embodiment, a standard DES algorithm and certain encryption keys which are stored in the SVC 20 and in the security module 78. All or selected portions of the separately encrypted data are then separately compared for confirmation purposes. In order to provide enhanced security a multiple encryption procedure is used...." The section continues with a description of the use of master keys et al.

In contrast, claim 15 of the present application requires at least the features of: *subdividing the input data into a plurality of data blocks*; loading the plurality of data blocks into a linear-feedback shift register for performing the program, the linear-feedback shift register having at least one non-linear function cryptographically enhanced using at least one downstream counter; *introducing at least one additional feedback into the linear-feedback shift register following the at least one downstream counter*; and *switching off the at least one additional feedback after a predefined first number of pulses of an associated clock.* The Davis reference at cols. 7 and 10 did not identically disclose each of these features in the manner presented in claim 15. Instead, the Davis reference appears to concern a different security feature as shown above in some of the recited passages from the Davis reference.

Accordingly, Applicants respectfully submit that claim 15 is allowable over the cited art. Further, claim 24 recites certain features analogous to those of claim 15 and is therefore allowable for essentially the same reasons as claim 15. The remaining claims 16 to 23 and 25 to 29 depend from one of claims 15 and 24, and are therefore allowable for at least the same reasons and the respective base claim.

Accordingly, Applicants respectfully request withdrawal of the rejection of claims 15 to 29 under 35 U.S.C. § 102(e) over the Davis reference.

CONCLUSION

In view of all of the above, it is believed that the rejection of claims 15 to 29, under 35 U.S.C. § 102(e), should be reconsidered and withdrawn, and that the currently pending claims are allowable. It is therefore respectfully requested that the present application issue.

The Examiner is respectfully encouraged to contact the undersigned via telephone if such communication might advance allowance of the present application.

Respectfully submitted,

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Dated: Nov. 10, 2005

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